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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/487,259		Sasaki Shigeyuki	1035-243	2949

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/487,259	Applicant(s) SHIGEYUKI, SASAKI
	Examiner Anh D. Mai	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *6-8 and 20-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 9-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election

1. Applicant's election without traverse of species of Embodiment #1, claims 1-5 and 9-19 in Paper No. 9 is acknowledged.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on October 24, 2001 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3-5, 9, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi et al. (JP 63-117445A).

Mutsumi teaches a manufacturing method for a semiconductor device as claimed including the steps of:

semi-full dicing a semiconductor wafer (1) so as to leave a dicing residual portion with a predetermined thickness between devices on the semiconductor wafer;

forming a protective layer (3) having a chemical etching resistant property on an element formation face of the semiconductor wafer; and

chemically etching the semiconductor wafer having the protective layer formed on the element formation face from the rear face side so as to polish the rear face of the semiconductor wafer, so as to remove the dicing residual portion to divide the semiconductor wafer into individual semiconductor chips, and so as to remove damaged areas in a cut face of the semiconductor wafer resulting from the semi-full dicing process. (See Figs. 2a-f).

With respect to the limitation: "*so as* to remove damaged areas in a cut face of the semiconductor wafer resulted from the semi-full dicing process". Mutsumi also chemically etches the semiconductor wafer (1) having the protective layer, thus the etching also remove the damaged areas. Furthermore, it appears that the protective layer (3) is only applied to the top surface of the semiconductor wafer (1). Therefore, the removal step of the process of Mutsumi '445 which includes removing the back side of the wafer more than the residual (6), also results in a removal of the damaged areas caused by the semi-full dicing. (See translation).

With respect to claim 3, the process of Mutsumi further includes: removing the protective layer (3) from the semiconductor chips after the chemical etching step.

With respect to claim 4, the semi-full dicing step of Mutsumi includes: subjecting the semiconductor wafer to semi-full dicing from the element formation face so as to leave a dicing residual portion (6) with a predetermined thickness on the rear face side of the semiconductor wafer.

With respect to claim 5, the protective layer (3) of Mutsumi is formed on the element formation face of the semiconductor wafer.

With respect to claim 9, the protective layer (3) is a film.

With respect to claim 13, the protective layer (3) of Mutsumi is further held with a uniform tension during the chemical etching step.

With respect to claim 14, the uniform tension of Mutsumi is maintained on the protective layer (3) by a protective holding means (7) placed on the surface of the protective layer (3) opposite the surface on which the semiconductor wafer (1) is affixed.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi '445 as applied to claim 1 above, and further in view of applicant admitted prior art (JP. 07-022358).

Mutsumi teaches all of the features of the claim with the exception of explicitly disclosing a testing step prior to form the semi-full dicing.

However, the admitted prior art disclosing that testing by probing to identify the working and non-working dices are routinely performed prior to the dicing the wafer into individual chips.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to perform testing prior to semi-full dicing the semiconductor wafer (1) of Mutsumi as taught by the admitted prior art to identify the bad chips prior to dicing.

5. Claims 10-13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi '445 as applied to claim 1 above, and further in view of Applicant admitted prior art, Kazuya (JP 07-022358).

With respect to claim 10, the protective layer (3) of Mutsumi is a chemical etching resistant film.

Thus, Mutsumi is shown to teach all the features of the claim with the exception of explicitly using an ultraviolet separation type.

However, '358 teaches using an ultraviolet separation, chemical etching resistant type film for the protective layer in a wafer dicing process, which the adhesive strength is reduced upon irradiated with ultraviolet rays.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the protective layer of Mutsumi using the ultraviolet separation type film as taught by '359 because the chemical etch resistant ultraviolet type film reduces it adhesive power under ultraviolet irradiation, hence easy removal of the dice.

With respect to claim 11, Mutsumi '445 and Kazuya '358 teach all of the features of the claim with the exception of using chemical etching resistance protective film having a characteristic of reduction adhesive strength upon application of heat. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use chemical etching resistance film of a thermal foaming type for the protective layer, since it has been held to be within the general skill of worker in the art to select a known material on the basis of it suitability for the intended use as a mater of obvious design choice. *In re Leshin, 125 USPQ 416.*

With respect to claim 12, the protective layer of Kazuya '358 comprises a chemical etching resistance film of sticking type, which has an adhesive strength as claimed.

With respect to claim 13, the protective layer (4) of Kazuya '358 is further held with an uniform tension.

With respect to claim 15, the uniform tension of Kazuya '358 is maintained on the protective layer (4) by a protective holding means (5) placed on the same surface of the protective layer (3) as the semiconductor wafer (3).

With respect to claim 16, the protective holding means (5) of Kazuya '358 having a chemical etching resistance property is placed on a peripheral portion of the protective layer (4) so as to surround the entire circumference of the semiconductor wafer (3).

With respect to claim 17, the protective layer holding means (5) of Kazuya '358 has a ring shape with a flat bonding face for bonding with the protective layer (4).

With respect to claim 18, Mutsumi and Kazuya '358 teach all of the features of the claim with the exception of explicitly disclosing a draining means.

However, the dicing apparatus is known to includes dicing wheel and cooling means to cool the wheel and removing the dust created during the cut. Water or liquid are known cooling medium. Therefore, standing liquid in the dicing apparatus must be eliminate to prevent contamination. Thus, draining means is inherent of the apparatus.

With respect to claim 19, as best understood by examiner, the radial shape of the draining means does not a appears to be critical since it is only to be used to drain the liquid.

6. Claims 10-13 and 15-17 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi '445 as applied to claim 1 above, and further in view of Usami et al. (U.S. Patent No. 5,893,746).

With respect to claims 10 and 11, Mutsumi teaches all of the features of the claim with the exception of including element which reduces the adhesive strength upon exposing to UV or heat.

However, Usami teaches using protective layer comprising elements which reduce adhesive strength upon exposing to UV or heat.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the protective layer (3) of Mutsumi using the elements as taught by Usami for easy removal of the diced chips.

With respect to claim 12, the protective layer of Usami comprises sticking type, which has an adhesive strength similar as claimed.

With respect to claim 13, the protective layer (4) of Usami is held by a protective layer holding means (101) with an uniform tension.

With respect to claim 15, the uniform tension of Usami is maintained on the protective layer (107) by a protective holding means (101) placed on the same surface of the protective layer (107) as the semiconductor wafer (105).

With respect to claim 16, the protective holding means (101) of Usami having a chemical etching resistance property is placed on a peripheral portion of the protective layer (107) so as to surround the entire circumference of the semiconductor wafer (105).

With respect to claim 17, the protective layer holding means (101) of Usami has a ring shape with a flat bonding face for bonding with the protective layer (107).

Response to Arguments

7. Applicant's arguments filed October 20, 2001 have been fully considered but they are not persuasive.

Regarding JP. 63-117445:

Applicant argues that when wax get into the grooves between the chip, the sides of the chip damaged by dicing cannot be etched by etchant.

However, '445 clearly discloses: "[W]ax 3 is applied so as to protect the surface of the IC wafer 1 from the etchant 4" (See translation page 2); and "[U]pon dicer test, cracks occur from these irregularities, and these cracks are developed by the machining distortions. Therefore, the chips after the dicing process is immersed in an etchant 4 so that the machining-affected layer is removed so as to form a smooth surface". (See translation page 4).

Contrary to Applicant's assertion, there is no "wax get into the grooves between the chip" any where.

Since the etchant 4 of '445 polishing the rear face side of the wafer and forms a smooth surface of the machining-effected layer, the chemically etching of '445 met the claim limitation.

Since the arguments with respect to the dependent claims based on the presumption that claim 1 is allowable, which it is not, the rejections of the dependent claims thereof are maintained.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
July 26, 2002